REMARKS

Inventorship

The Application properly identifies the joint inventors.

Drawings

FIGs. 1 and 4 have been amended to include descriptive labels identifying the different controllers. No new matter has been added.

Specification

The title of the invention has been changed to the descriptive:

"Output-powered Over-voltage Protection Circuit".

The abstract has been modified to eliminate "legal phraseology".

Claim Rejections - 35 USC § 102

Claims 1-15 are pending in the present Application. With this Response, Applicants have amended Claims 1, 2, 5, 9, 12, and 14, and canceled Claims 3, 4. The amendments to the claims are expressed in the detailed listing above.

Claims 1-8, 12, and 13 are rejected under 35 U.S.C. 102(a) as being anticipated by prior art reference publication "Maxim Integrated products – CPU Step-Down Controller (IMVP-II) (MAX1718)" (hereafter "Maxim").

Amended Claim 1 recites:

1. (Currently amended) A circuit for providing a regulated voltage comprising:
a switching voltage regulator, comprising:

an upper transistor connected to an input voltage from a voltage source, the upper transistor having a control terminal;

a lower transistor connected to the upper transistor, the lower transistor having a control terminal; and

a voltage regulator controller connected to receive the regulated voltage, the voltage regulator controller operable to generate a first control signal applied to the control terminal of the upper transistor, and further operable to generate a second control signal applied to the control terminal of the lower transistor; and

a voltage protection circuit comprising:

an over-voltage detector circuit powered by the regulated output voltage operable to detect an over-voltage condition and further operable to generate an over-voltage detected signal, wherein the over-voltage detected signal causes the lower transistor to draw sufficient current from the voltage source such that the over-voltage condition is abated.

The Examiner identifies feedback line (FB) in FIG. 2 (p. 13) as satisfying the limitation: "an over-voltage detector circuit powered by the regulated output voltage".

Applicant respectfully traverses this rejection. Maxim's over-voltage detector circuit includes the OVP/UVP DETECT block and the connected two logic gates driving the DL terminal of the lower transistor. As clearly seen, the second of the logic gates is driven by a V_{DD} supply voltage. On page 2 and 3 the V_{DD} output voltage is described as being in the range of 4.5-5.5 Volt. Even if the over-voltage detector circuit is narrowly interpreted as the OVP/UVP DETECT block, Maxim does not indicate explicitly the voltage supply for that block. The standard practice in documenting circuit layouts is that regular voltage supply lines, such as a V_{DD} line are not shown explicitly. However, non-standard voltage supply lines, such as supply coming from the output terminal are expected to be shown. Note, that the FB line is connected to the OVP/UVP DETECT block, but it provide a detected signal and not a voltage supply.

In contrast, Applicant's over-voltage detector circuit is powered by the regulated output voltage. To clarify that the original application's "regulated voltage" is in fact the output voltage, Claim 1 has been amended to recite:

an over-voltage detector circuit powered by the regulated output voltage.

This distinction is important, as in certain failure modes of the protection circuit the power supply may fail to provide a V_{DD} voltage with a sufficiently high level. The protection circuit of Maxim stops functioning without an adequate V_{DD}, thus possibly outputting an unacceptably high output voltage.

In contrast, Applicant's protection circuit is powered by the regulated output voltage. Therefore, even if a sufficient V_{DD} voltage is not supplied, Applicant's protection circuit continues providing an acceptable output voltage.

Claims 2-8 depend on allowable Claim 1, and are therefore allowable themselves.

Claims 9, 14, and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Lorincz et al.

The Examiner identifies the "over-voltage detector" as comparator 21 of Lorincz, powered by a regulated voltage. Applicants respectfully traverses this rejection.

Comparator 21 of Lorincz is powered from supply line 11. As such, comparator 21 is not powered by the regulated output voltage. To clarify that the "regulated voltage" is in fact the regulated output voltage, Applicant amended Claim 9 to recite:

"an over-voltage detector powered by a regulated output voltage operable to generate an over-voltage detected signal"

Claims 12 and 14 have been amended to recite a

"an over-voltage detector powered by a regulated output voltage"

as well.

For at least the above reasons, all pending Claims 1-3, and 6-15, as amended, are not anticipated by the Maxim circuit.

Claim Rejections - 35 USC § 103

Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lorincz et al in view of Koelling et al. Applicants respectfully traverses this rejection.

As stated by the Examiner, Koelling describes that a possible embodiment of the over-voltage detector can be "a self-regulating bandgap detector". This embodiment does not modify in any sense Applicant's argument that Lorincz's over-protection circuit is not "powered by the regulated output voltage", but by a regular voltage supply. In particular, the Examiner does not provide any argument to show that Koelling's band gap detector would be powered by the output voltage. Indeed, Koelling powers his transistors with a V_{DD} voltage, as shown e.g. in FIGs. 4-6. As Claims 10 and 11 depend from the allowable independent Claim 9, Claims 10 and 11 are allowable as well.

CONCLUSION

For at least the above reasons, Applicants respectfully request that the pending claims be allowed and the case passed to issue. Should the Examiner wish to discuss the Application, it is requested that the Examiner contact the undersigned at (415) 772-1200.

EXPRESS MAIL LABEL NO.:
EV 305 257 355 US

Respectfully submitted,

By:

Gergely T. Zimányi
Agent of Record
Registration No. 45,754
GTZ/rp

October 9, 2003

SIDLEY AUSTIN BROWN & WOOD LLP
555 California Street, Suite 5000
San Francisco, CA 94104-1715
(415) 772-1200